

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-14. (Cancelled)

15. (Currently amended) A MOSFET circuit comprising:

- a first MOS transistor having a first number of cells,
- a second MOS transistor having a second number of cells, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and
- a Zener diode coupled between a gate of the first MOS transistor and a gate of the second MOS transistor, wherein the Zener diode is further coupled between the gate of the second MOS transistor and a control input of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second MOS transistor.

18. (Previously presented) The MOSFET circuit as claimed in claim 19, further comprising a second resistor connected in series with a parallel circuit formed by the Zener diode and the first resistor.

19. (Previously presented) The MOSFET circuit as claimed in claim 15, further comprising a first resistor connected in parallel with the Zener diode.

20. (Previously presented) The MOSFET circuit as claimed in claim 19, wherein the Zener diode and the first resistor are integrated with one another.

21. (Previously presented) The MOSFET circuit as claimed in claim 20, wherein the Zener diode and the first resistor are formed by a highly doped polycrystalline layer of a first conduction type and a polycrystalline layer of a second conduction type that is in contact with the highly doped polycrystalline layer.

22. (Previously presented) The MOSFET circuit as claimed in claim 21, wherein the polycrystalline layer of the second conduction type is located on a polysilicon gate plane of the MOSFET circuit.

23. (Previously presented) The MOSFET circuit as claimed in claim 21, wherein a doping concentration of the highly doped layer is less than 10^{19} charge carriers cm^{-3} .

24. (Currently amended) A MOSFET circuit comprising:

- a first MOS transistor having a first number of cells, the first MOS transistor integrated into a semiconductor body;
- a second MOS transistor having a second number of cells, the second MOS transistor integrated into the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and reference potential, and
- a Zener diode coupled between a gate of the first MOS transistor and a gate of the second MOS transistor, wherein the Zener diode is further coupled between the gate of the second MOS transistor and a control input of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second MOS transistor.

25. (Previously presented) The MOSFET circuit as claimed in claim 24, wherein the first number of cells is at least twice the second number of cells.

26. (Previously presented) The MOSFET circuit as claimed in claim 25, wherein the first number of cells is at least ten times the second number of cells.

27. (Previously presented) The MOSFET circuit as claimed in claim 25, wherein the first number of cells is approximately 1000.

28. (Previously presented) The MOSFET circuit as claimed in claim 24, wherein the first MOS transistor and the second MOS transistor comprise CoolMOS transistors.

29. (Previously presented) The MOSFET circuit as claimed in claim 24, wherein the semiconductor body is of a second conduction type and charge compensation regions of a first conduction type are incorporated into the semiconductor body.

30. (Currently amended) An integrated MOSFET circuit comprising:

- a first MOS transistor having a first number of cells, said transistor being integrated in a semiconductor body,
- a second MOS transistor having a second number of cells, said transistor being integrated in the semiconductor body, the second number being less than the first number and the second MOS transistor being provided with a source-drain path in parallel with a source-drain path of the first MOS transistor between a voltage source and a reference potential, and
- a Zener diode connected between a gate of the first MOS transistor and a gate of the second MOS transistor, said Zener diode comprising a polycrystalline layer on a polycrystalline gate plane of the first and second MOS transistors and a zone provided in the polycrystalline layer and having an opposite conduction type to a conduction type of the polycrystalline layer, wherein the Zener diode is further coupled between the gate of the second MOS transistor and a control input of the MOSFET circuit, and wherein the Zener diode is forward biased from the control input to the gate of the second MOS transistor.

31. (Previously presented) The integrated MOSFET circuit as claimed in claim 30, further comprising a resistor connected in parallel with the Zener diode, the resistor formed by the pn junction between the polycrystalline layer and the zone.

32. (Previously presented) The integrated MOSFET circuit as claimed in claim 31, wherein the doping concentration of the zone is less than 10^{19} charge carriers cm^{-3} .

33. (Previously presented) The MOSFET circuit as claimed in claim 30, wherein the first number of cells is at least twice the second number of cells.

34. (Previously presented) The MOSFET circuit as claimed in claim 30, wherein the first number of cells is at least ten times the second number of cells.

35. (Cancelled)